

## CLAIMS

What is claimed is:

Sub  
A<sup>3</sup>

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	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2
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1. An apparatus comprising:

- a configuration storage containing configuration parameters to configure a processor in one of a normal execution mode and an isolated execution mode;
- an access generator circuit coupled to the configuration storage to generate an isolated access signal using at least one of the configuration parameters and access information in a transaction, the isolated access signal being asserted when the processor is configured in the isolated execution mode; and
- a bus cycle decoder coupled to the access generator circuit to generate an isolated bus cycle corresponding to a destination in the transaction using the asserted isolated access signal and the access information.

1           2.     The apparatus of claim 1 wherein the configuration parameters include an  
2     isolated setting and an execution mode word.

3. The apparatus of claim 1 wherein the destination in the transaction is one of an isolated memory area in a memory external to the processor, an isolated register, and an isolated state.





1           15.     The apparatus of claim 13 wherein the logical processor withdrawal from  
2     the isolated state updates a logical processor counter in the chipset in a second direction.

1           16.     A method comprising:

2                 configuring a processor in one of a normal execution mode and an isolated  
3     execution mode using a configuration storage in the processor, the configuration storage  
4     containing configuration parameters;

5                 asserting an isolated access signal by an access generator circuit using at least one  
6     of the isolated area parameters and access information in a transaction when the processor  
7     is configured in the isolated execution mode; and

8                 generating an isolated bus cycle corresponding to a destination in the transaction  
9     by a bus cycle decoder using the asserted isolated access signal and the access  
10    information.

1           17.     The method of claim 16 wherein the configuration parameters include an  
2     isolated setting and an execution mode word.

1           18.     The method of claim 16 wherein the destination in the transaction is one of  
2     an isolated memory area in a memory external to the processor, an isolated register, and  
3     an isolated state.





1           30.     The method of claim 28 wherein the logical processor withdrawal from the  
2 isolated state updates a logical processor counter in the chipset in a second direction.

1           31.     A system comprising:

2           a chipset;

3           a memory coupled to the chipset having an isolated memory area; and

4           a processor coupled to the chipset and the memory having an isolated bus cycle  
5 generator, the isolated bus cycle generator comprising:

6                     a configuration storage containing configuration parameters to  
7                     configure the processor in one of a normal execution mode and an isolated  
8                     execution mode,

9                     an access generator circuit coupled to the configuration storage to  
10                    generate an isolated access signal using at least one of the isolated area  
11                    parameters and access information in a transaction, the isolated access  
12                    signal being asserted when the processor is configured in the isolated  
13                    execution mode, and

14                    a bus cycle decoder coupled to the access generator circuit to  
15                    generate an isolated bus cycle corresponding to a destination in the  
16                    transaction using the asserted isolated access signal and the access  
17                    information.

1           32.     The system of claim 31 wherein the configuration parameters include an  
2 isolated mode value and an execution mode word.

1           33.     The system of claim 31 wherein the destination in the transaction is one of  
2 the isolated memory area, an isolated register, and an isolated state.

1           34.     The system of claim 33 wherein the access information includes a physical  
2 address and an access type.

1           35.     The system of claim 34 wherein the configuration storage comprises:  
2                   a register to contain the isolated setting for defining the isolated memory area.

1           36.     The system of claim 35 wherein the isolated setting is one of a mask value,  
2 a base value, and a length value.

1           37.     The system of claim 36 wherein the configuration storage further  
2 comprises:

3 a processor control register to contain the execution mode word, the execution  
4 mode word being asserted when the processor is configured in the isolated execution  
5 mode.

1 38. The system of claim 37 wherein the access generator circuit comprises:  
2 an address detector to detect if the physical address is within the isolated memory  
3 area defined by the isolated setting.

1 39. The system of claim 38 wherein the isolated bus cycle is one of a data  
2 access cycle, a control access cycle, and a logical processor access cycle.

1 40. The system of claim 39 wherein the data access cycle is generated when  
2 the access type is a memory reference to the isolated memory area.

1 41. The system of claim 39 wherein the isolated register is in a chipset  
2 external to the processor.

1 42. The system of claim 41 wherein the control access cycle is generated when  
2 the access type is an input/output reference to the isolated register.

